

SHEET INDEX

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SYMBOL
BUFFER A
ELEMENT 1001
A

TERM. MOD	FUNCTION	TERM.	LOC	TERM. MOD	FUNCTION	TERM.	LOC
ACK10	I	308	247	-INF120	0	215	3H7
BLK.CB1	I	005	348	INF130	0	306	3H9
BLK.FLD	I	2070	349	INF140	0	204	3H9
SND	I	004	248	INF150	0	300	3H2
RDY-YD	I	304	243	INTP0	0	017	2H8
CLK	I	305	247	INTP1	0	013	2H5
GPR0	I	C19	246	LRAD0	0	003	2H5
TAUTO	I	208	349	LRAD1	0	100	2H6
INF000	I	013	241	ROY0	0	205	2H0
INF010	I	113	241	RT.ADR0	0	003	2H5
INF020	I	014	241	RT.ADR0	0	100	2H6
INF030	I	114	241	RT.ADR0	0	062	2H6
INF040	I	012	241	ST.CLK0	0	108	2H1
INF050	I	112	240	STUFF0	0	212	3H6
INF060	I	217	347	SH01	0	019	3H4
INF100	I	216	347	STED0	0	103	2H2
INF110	I	011	346	TG-SEQ1	0	010	3H5
INF120	I	313	346	UNL-BAD0	0	201	3H6
INF130	I	209	346	WLT0	0	019	3H4
INF140	I	106	340	+5	P	000,119	2H2
INF150	I	004	340	GRO	0	200,119	2H4
INT0	I	107	241				
LOCKED	I	318	246				
PE1	I	001	240				
RCD	I	118	242				
R00	I	115	243				
S00	I	018	242				
S1-0	I	116	243				
STF100	I	104	342				
C3RT	I	105	349				
C3C0	I	209	341				
CLC11	I	008	341				
C3CF1	I	111	348				
DV.FILL1	I	110	3H0				
ENB0	I	109	3H5				
EM0	I	304	2H0				
GPO	I	117	2H6				
TOENO	I	016	2H8				
INF060	I	101	3H5				
INF070	I	102	3H5				
INF080	I	201	3H2				
INF090	I	315	3H8				
INF100	I	318	3H8				
INF110	I	214	3H8				

RECORD OF CHANGES

DRG. ISS.	PREV. FURN.	STO	HFR. DISC.	SEE NOTE

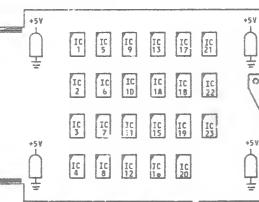
NOTES:

1. 1 GROUND RETURN2. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS3. BATTERY AND GROUND TERMINALS FOR
INTEGRATED CIRCUITS

IC CODE	BAT. CODE	GRD. CODE	TERM.
A1BC	16	7, 8	
A1BP	16	7	
A1BR	16	7, d	
A1CH	16	8	
A1CD	16	8	
A1CL	16	7, 8	
A1CK	16	8	
A1EG	16	7, 8	
A1EH	16	7, 8	
A1U	16	B	
A1M	16	8	

4. BATTERY AND GROUND TERMINALS FOR
THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRO	200,319

5. HORIZONTAL MOUNTING CENTERS AT
0.50 INCH.6. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)

UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

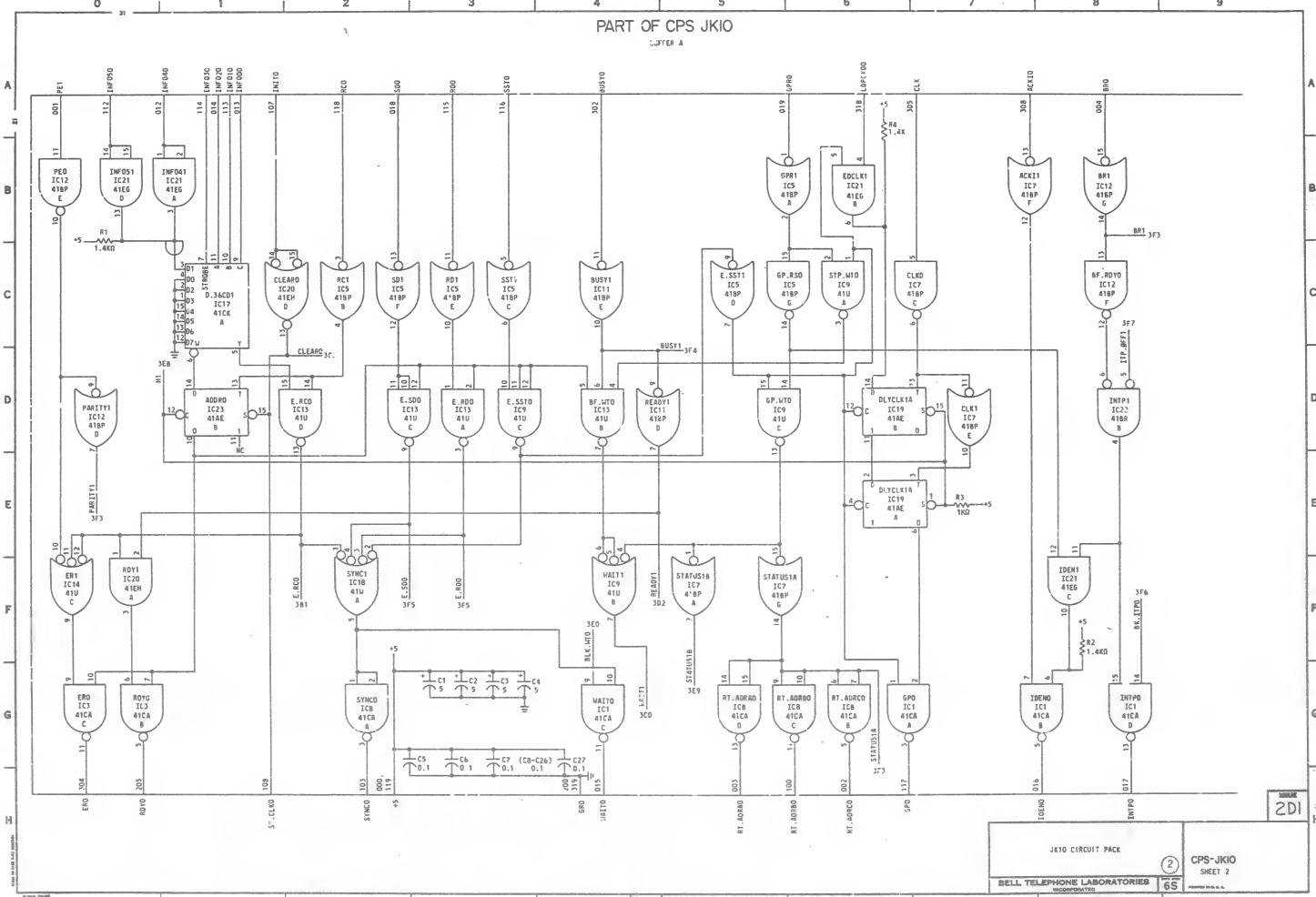
CATEGORY	NO.
CIRCUIT PACK CODE	JX10
CONNECTOR ON FRAME	947C
	DR
	947A
SERIES FOR LATEST CLASS A CHANGE (AND HIGHER SERIES IS ACCEPTABLE.)	
ACCEPTABLE SERIES	1

1. WHEN CHANGES ARE MADE IN THIS DRAWING
ONLY THOSE SHEETS AFFECTED WILL BE
RE-ISSUED.
2. THIS SHEET INDEX WILL BE RE-ISSUED AND
BROUGHT UP TO DATE EACH TIME ANY SHEET
OF THE DRAWING IS RE-ISSUED, OR A NEW
SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED
OR NEW SHEET WILL BE THE SAME ISSUE
NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN
THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET
INDEX IS RECOGNIZED AS THE LATEST ISSUE
NUMBER OF THE DRAWING AS A WHOLE.

NOTICE: NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL
SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.1W98
JX10 CIRCUIT PACKISSUE
2D1
AT&T CO
STANDARDBUFFER A
CIRCUIT
BELL TELEPHONE LABORATORIES
INCORPORATED
6SCPS-JK10
4 SHEETSCPS-JK10
4 SHEETS

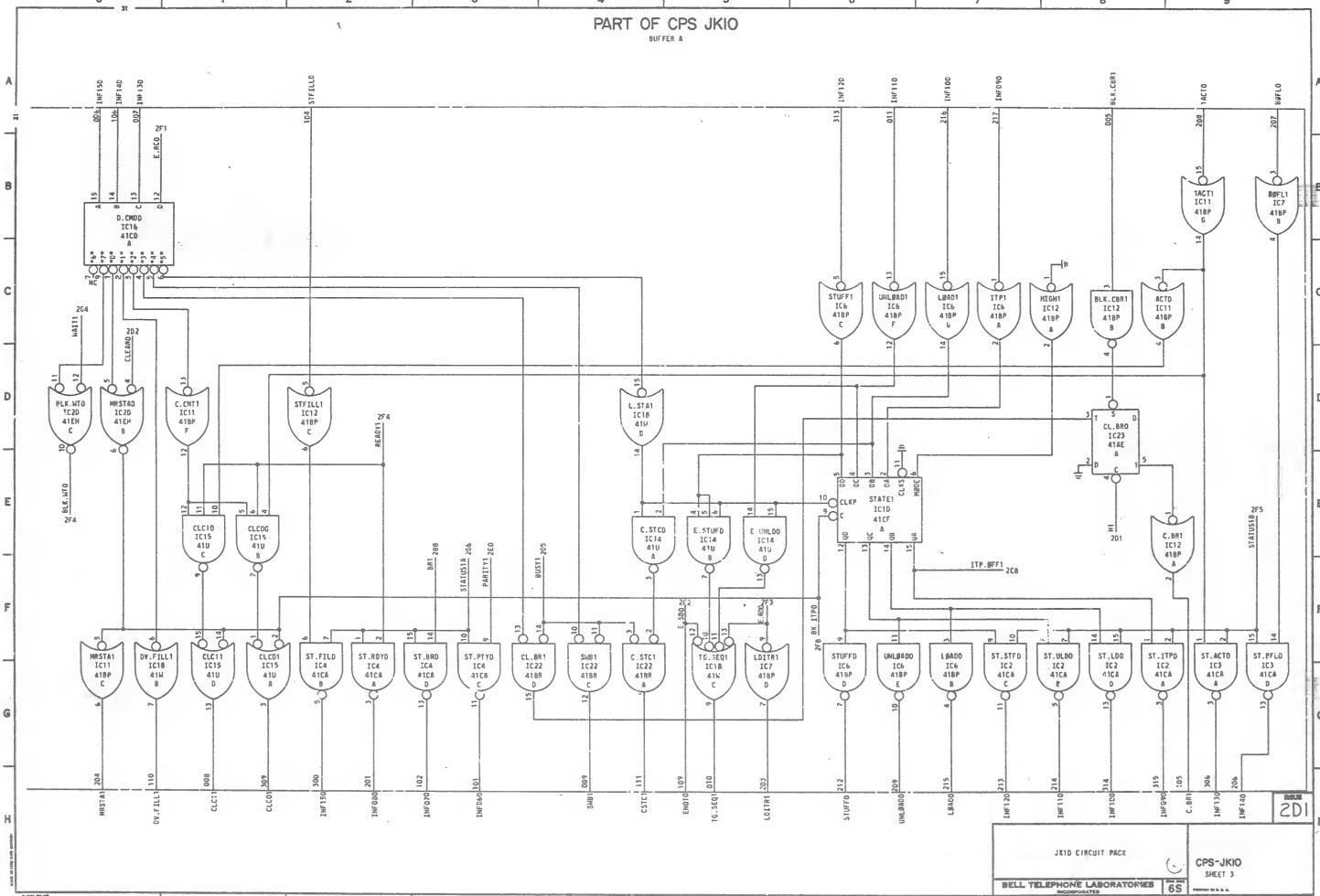
PART OF CPS JK10

LOTTER A



PART OF CPS JKIO

BUFFER A



PART OF CPS JK10

BUFFER A

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM	IC1 41CA	IC2 41CA	IC3 41CA	IC4 41CA	IC5 41BP	IC6 41BP	IC7 41BP	IC8 41CA	IC9 41U	IC10 41CF	IC11 41BP	IC12 41BP	
10	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	
A	SPO	266	ST. ITPO	368	ST. ACTD	369	ST. RYD	362	GPR1	286	ITP1	367	
B	IDENO	268	ST. ULDD	368	RDYD	260	ST. FILD	362	RC1	262	STATUS1	368	
C	WATD	264	ST. STFD	367	ERD	260	ST. PIYO	363	SC1	263	BFBL1	369	
D	INTPO	268	ST. LD ¹	368	ST. BFLD	369	ST. BRD	363	SST1	265	PT.ADRD	266	
E							E.SST1	265	STUFT1	266	RT.ADRD	266	
F							SD1	265	STUFT2	266	E.SST2	265	
G							SD1	265	CLK1	266	RT.GRD	265	
							SD1	265	CLK2	266	GP.WD	295	
							GP.RSD	266	CLK3	266			
								GP.RSD	266	CLK4	266		
								GP.RSD	266	CLK5	266		

LOC CODE ELEM	IC13 41U	IC14 41U	IC15 41U	IC16 41CD	IC17 41K	IC18 41M	IC19 41AE	IC20 41H	II 21 41E6	IC22 41BR	T _C 23 41Z	
10	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	E.RD0	203	C.SSTD	364	CLC01	361	D.CMD0	380	D.36CD1	2C1	SYNC1	2F2
B	BF.WTD	204	E.STFU	365	CLC00	361	DV.FILL1	360	DLCLK18	2E5	RG11	2F0
C	E.SBD	203	ERI	270	CLC10	361	TG.SEQ1	365	DLCLK18	2E6	IMP04	2B1
D	E.RCD	202	E.UHLD	365	CLC11	361	L.STA1	384	IMP05	2C2	CL.TC1	364
E										CL.BRD	363	
F										IMP06	2B1	
G										IMP07	2B1	
H										IMP08	2B0	

CAPACITOR

DESIG	CODE
[4] C1-C4	6018.5
[23] C5-C27	KS-19774 L5.D.1

RESISTOR

DESIG	CODE
[2] R1,R2	KS-20015 L1A.1,4K0
R3	KS-20016 L1A.1,4K0
R4	KS-200615 L1A.1,4K0

CIRCUIT DESCRIPTION

CIRCUIT PACK JK10 HANDLES THE BUFFER ADDRESS AND COMMAND DECODING AND HANDSHAKING ON THE COMMON PARALLEL BUS. THE BUFFER ADDRESS SECTION IS DECODED BY A 4-TO-16 DECODE-INPUT SEQUENCER DRIVEN BY JACCI1 CARRYING THE ADDRESS F/T. ADDRESS IS TO BE CLEARED ON THE LEADING EDGE OF RCD. SELECTING THE BUFFER ADDRESS SECTION BY SETTING RCD0. THE STATE REGISTER STUFF1 IS SET BY THE INPUT T. THE BUFFER IS DESELECTED (RCD0 IS SET) EITHER BY INPUT T OR BY AN RC ACCOMPANYING A WRITE CYCLE. THE BUFFER IS DESELECTED BY SETTING RCD1. SYNC1 IS asserted IN RESPONSE TO RCD, SBD, RCD, OR SSTD AND REGISTERS SYNC1 FOLLOWING THE REMOVAL OF THE COMMAND SIGNALS. END IS asserted ON THE REMOVAL OF THE RCD INPUT. END IS HELD TRUE ON A PARITY ERROR INDICATION (PE) TRUE.

THE RECEIPTION OF A SSTD1 TURNS STATUS INFORMATION INTO THE BUS AND ASSERTS WATD AND parity GENERATE REQUEST RPO IN ADDITION TO SYNC1. THE NEXT FALLING EDGE OF CLK SETS DLCLK18 AND T' F FOLLOWING RISING EDGE SETS DLCLK18, CTT1, AND T' G. THE PARITY CHECKER IS ASSERTED ON THE BUS TERMINATOR RESPOND BY ASSERTING GRD WHICH REMOVES STATUS INFORMATION FROM THE BUS AND INHIBITS THE BUFFER WATD. THE DELAY CHAIN IS CLEARED WHEN SSTD1 IS REMOVED.

RCD CLEARS INFORMATION ON THE PARALLEL BUS INTO THE INTERFACED TRANSFER REGISTER, ITK, ON J12 VIA LEAD LOT15. ITK IS CLEARED ON THE 17TH CYCLE OF THE BUS LEAD INPUT. RCD0 IS ASSERTED WHEN SYNC1 IS ACTIVE AND THE BUFFER IS SELECTED AND MAY BE BLOCKED BY CTT1 AND T' G. THE DECODER (O.CMD0) OUTPUT 7, T'GPO IS ASSERTED WHEN RCD IS ACTIVE AND THE STATE REGISTER TIP1TIP2 BIT IS NOT SET. An INTERRUPT CONDITION ENABLES BUFFER INTERRUPT IDENTIFICATION GATE IDENT IN RESPONSE TO AN ACKED COMMAND.

O.CMD0 DECODES THE INFORMATION ON INF130-IMP150 WHEN ACO IS ON TO ACTIVATE 1 OUT OF 8 DECODER OUTPUTS. OUTPUT 7 PREVIOUSLY MENTIONED IS USED IN CONNECTION WITH A HOP COMMAND.

OUTPUT 5CLOCKS THE BIT PATTERN ON LEADS IMP90-IMP120 INTO THE STATE REGISTER STUFF1. THE STATE REGISTER CONTROLS THE STATES OF LEADS STUFF1, UNLBD0, LBD0, INT, FF1, WHICH INDICATE THE TYPE OF OPERATION TO BE PERFORMED ON THE OFF-LINE BUFFER. OUTPUT 4 ASSERTS SAB1. THIS IS THE ACT OF THE STATE REGISTER REQUESTING THE BUFFER. OUTPUT 3 CLOCKS THE CL.BRD F/F WHICH ASSERTS C.BR1, CLEARING THE SR FLIP-FLOP J111. CL.BRD F/F MAY BE SET BY AN ACTIVE LEVEL ON J111. CL.BRD F/F IS SET BY ASSERTING SAB1. THE CL.BRD BUFFER COUNTER IS INDICATED BY THE STATE OF JACT0. OUTPUT 1 ASSERTS DV.FILL1 RESULTING IN A CC-INITIATED OFF-LINE BUFFER FILL OPERATION. OUTPUT D ASSERTS BUFFER COUNTERS VIA CLCD0 AND CLC11, AND ASSERTING INTSTAT. OUTPUT 6 OF O.CMD0 IS NOT USED.

CLC11 CLEARS THE STUFF SEQUENCE COUNTER J111 WHILE THE LOAD BIT IN THE STATE REGISTER IS BEING SET. TG.SEQ1 STARTS OFF-LINE SEQUENCING ON J111 IF EITHER THE STATE REGISTER STUFF1 OR UNLBD 0:1 IS BEING SET OR IF RCD OR SBD IS ACTIVE.

D.CMD0 TRUTH TABLE

INF150	INF130	ASSIGNED OUTPUT
0 0	0 0	7
0 0	1 1	3
0 1	0 0	5
1 1	1 1	1
1 0	0 0	6
1 0	0 1	2
1 1	0 0	4
1 1	1 1	0

